

## Power MOSFET

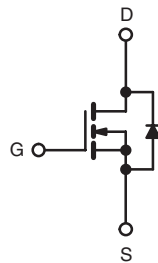
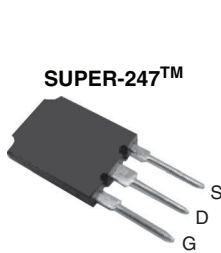
PRODUCT SUMMARY		
$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.16
$Q_g$ (Max.) (nC)	220	
$Q_{gs}$ (nC)	64	
$Q_{gd}$ (nC)	110	
Configuration	Single	

### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Lead (Pb)-free Available



**RoHS\***  
COMPLIANT



N-Channel MOSFET

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

ORDERING INFORMATION	
Package	Super-247™
Lead (Pb)-free	IRFPS30N60KPbF
	SiHFPS30N60K-E3
SnPb	IRFPS30N60K
	SiHFPS30N60K

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	600	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	30	A
		$T_C = 100$ °C	19	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	120		
Linear Derating Factor		3.6	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	520	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	30	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	45	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	450	W
Peak Diode Recovery $dV/dt^c$		$dV/dt$	13	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	

#### Notes


- Repetitive rating; pulse width limited by maximum junction temperature.
- Starting  $T_J = 25$  °C,  $L = 1.1$  mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 30$  A.
- $I_{SD} \leq 30$  A,  $dI/dt \leq 630$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain) <sup>a</sup>	$R_{thJC}$	-	0.28	

### Note

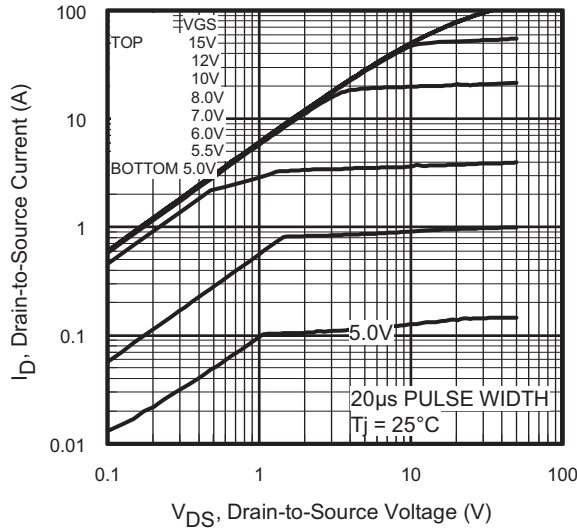
a.  $R_{th}$  is measured at  $T_J$  approximately 90 °C.

SPECIFICATIONS $T_J = 25\text{ °C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1\text{ mA}^d$		-	0.66	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	50	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 18\text{ A}^b$	-	0.16	0.19	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 18\text{ A}$		16	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$		-	5870	-	pF
Output Capacitance	$C_{oss}$			-	530	-	
Reverse Transfer Capacitance	$C_{rss}$			-	54	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	6920	-	pF
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	140	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}, V_{DS} = 480\text{ V}^b$	-	-	220	nC
Gate-Source Charge	$Q_{gs}$			-	-	64	
Gate-Drain Charge	$Q_{gd}$			-	-	110	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 30\text{ A},$ $R_G = 3.9\text{ }\Omega, V_{GS} = 10\text{ V}^b$		-	29	-	ns
Rise Time	$t_r$			-	120	-	
Turn-Off Delay Time	$t_{d(off)}$			-	56	-	
Fall Time	$t_f$			-	50	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	30	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	120	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ °C}, I_S = 30\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ °C}, I_F = 30\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	640	960	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	11	16	$\mu\text{C}$
Body Diode Recovery Current	$I_{RRM}$			-	31	-	A
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

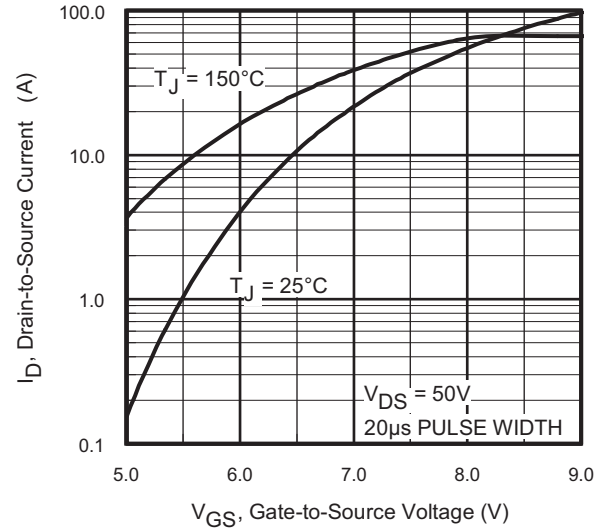
### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$ .

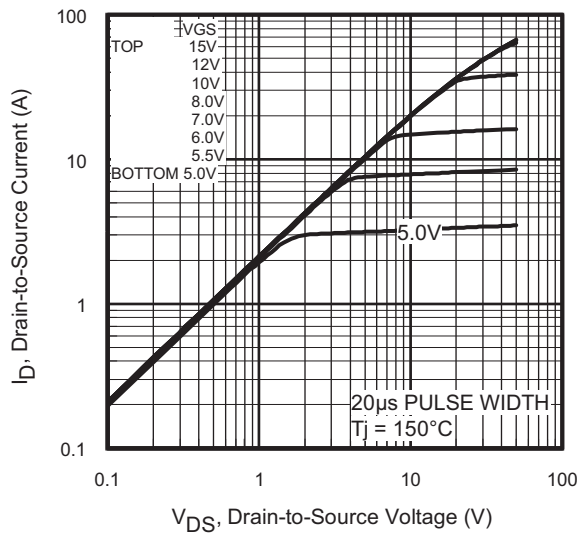
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



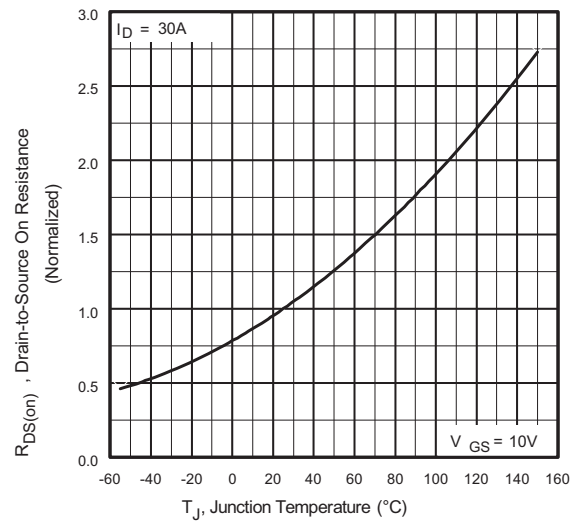
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

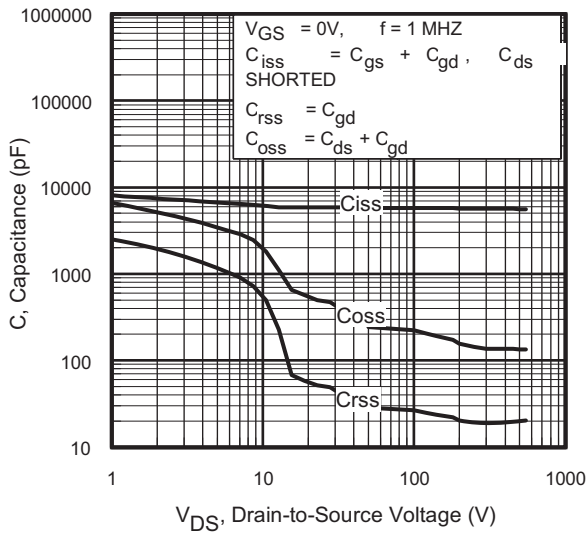


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

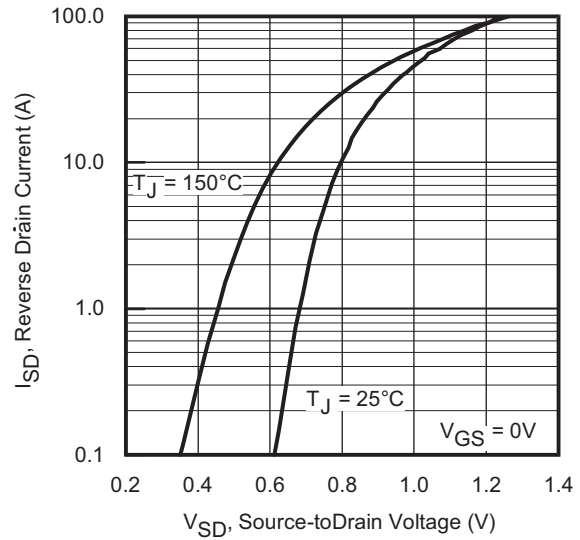


Fig. 7 - Typical Source-Drain Diode Forward Voltage

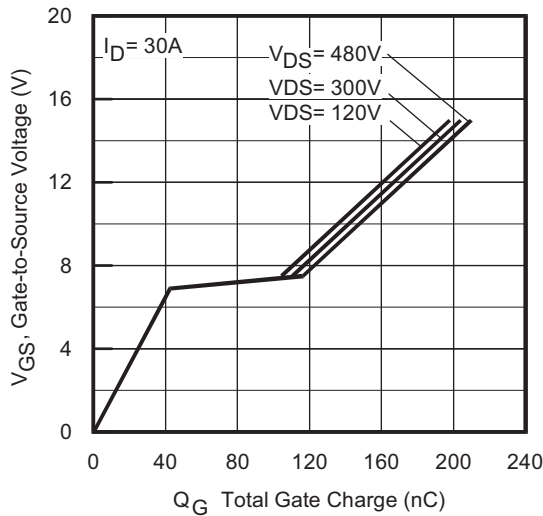


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

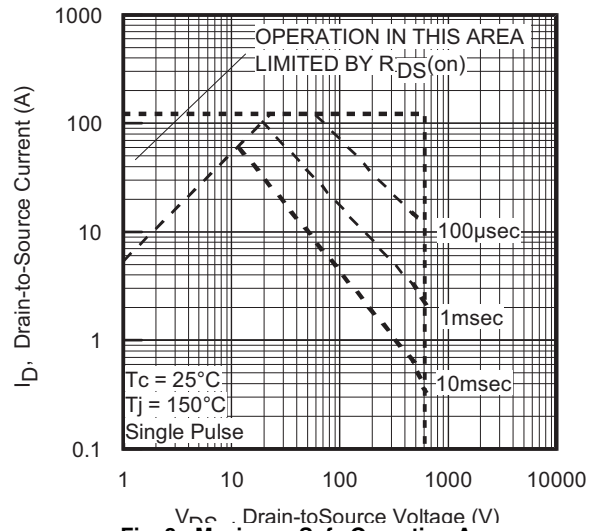
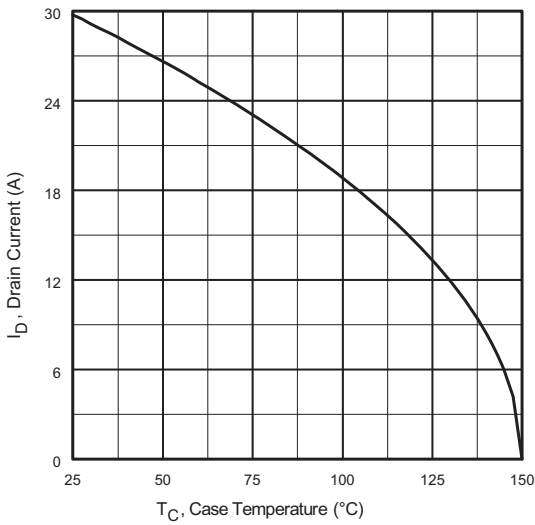
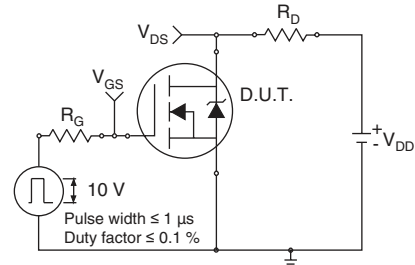


Fig. 8 - Maximum Safe Operating Area



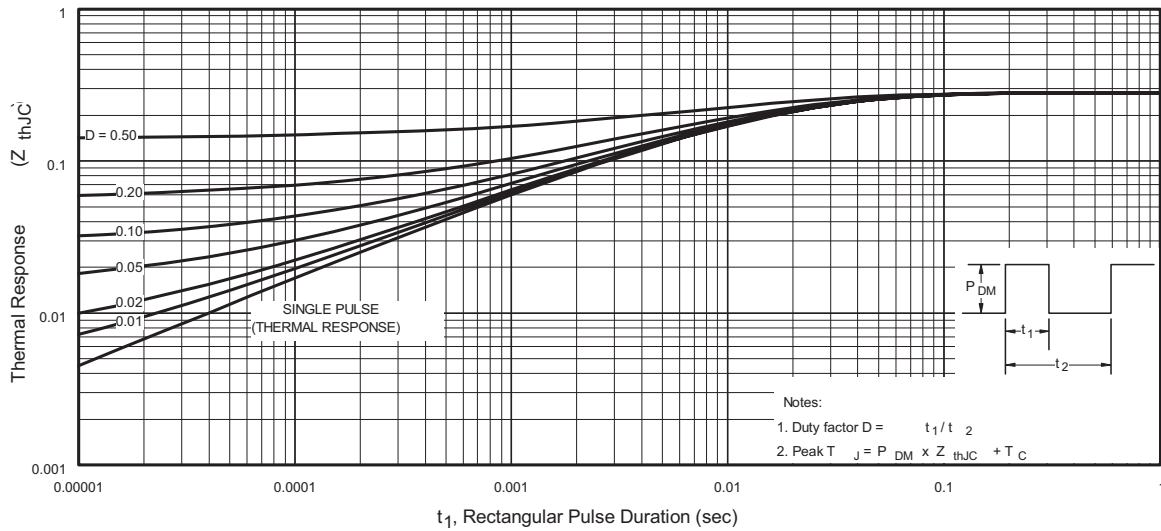
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

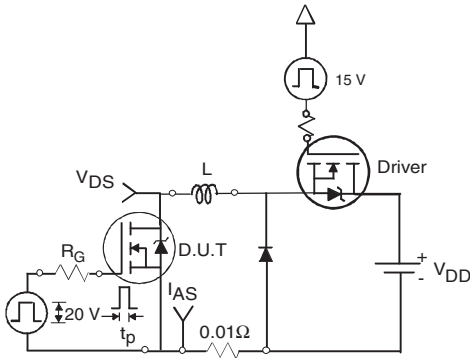


Fig. 12a - Unclamped Inductive Test Circuit

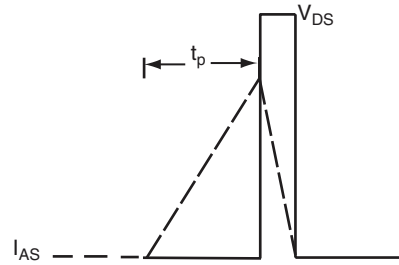


Fig. 12b - Unclamped Inductive Waveforms

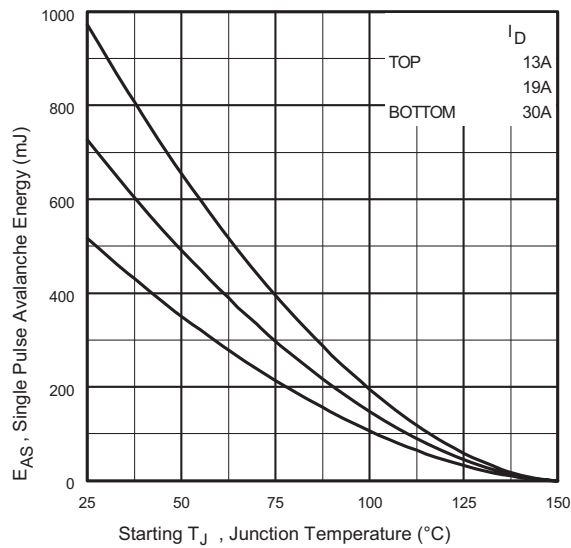


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

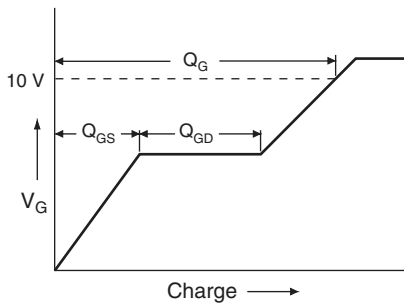


Fig. 13a - Basic Gate Charge Waveform

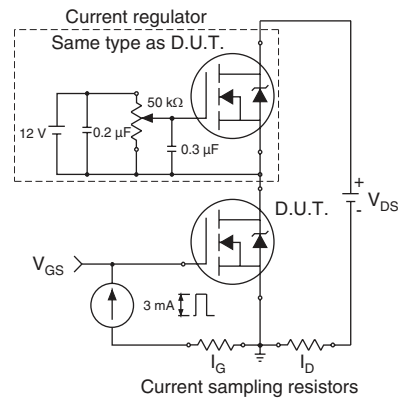
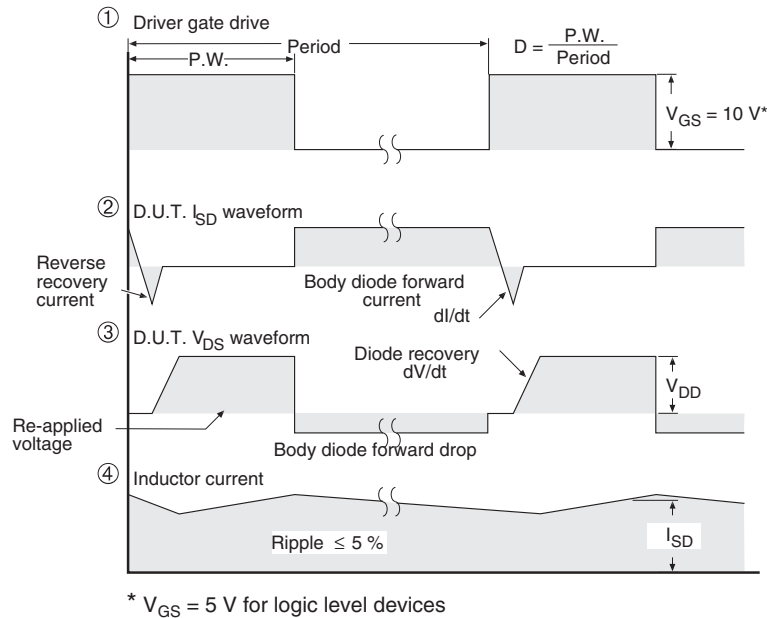
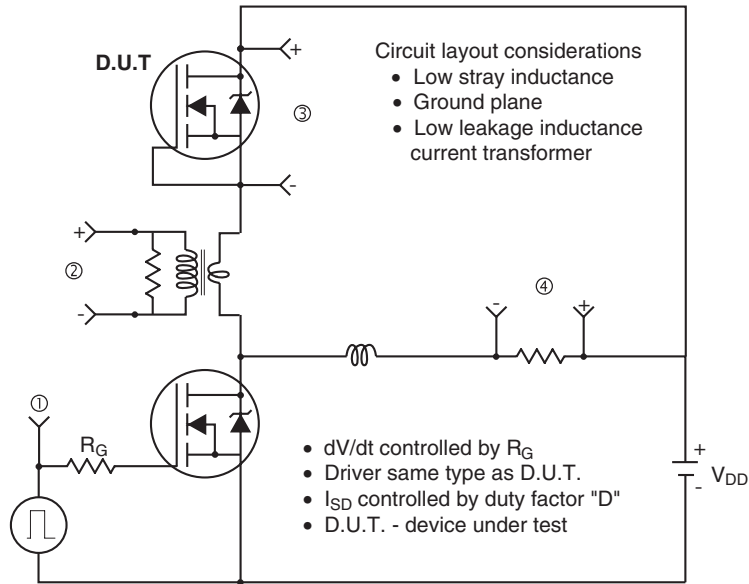


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery $dV/dt$ Test Circuit



**Fig. 14 - For N-Channel**

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